

CLAIMS

WHAT IS CLAIMED IS:

- 1 1. An integrated circuit comprising:
2 a first wafer including a silicon germanium layer, a strained
3 silicon layer, and a first insulating layer; and
4 a second wafer including a substrate and a second insulating
5 layer, the second insulating layer being attached to the first insulating layer.
- 1 2. The integrated circuit of claim 1, wherein the substrate is a bulk
2 semiconductor substrate.
- 1 3. The integrated circuit of claim 2, wherein the silicon germanium
2 layer includes a hydrogen breaking interface.
- 1 4. The integrated circuit of claim 1, wherein a channel region is
2 disposed in the strained silicon layer.
- 1 5. The integrated circuit of claim 4, wherein a source region and a
2 drain region are disposed in the strained silicon layer.
- 1 6. The integrated circuit of claim 5, wherein an aperture is formed
2 in the silicon germanium layer to expose the strained silicon layer.
- 1 7. The integrated circuit of claim 6, wherein a gate structure is
2 provided in the aperture.
- 1 8. A multilayer structure containing a plurality of SMOS
2 transistors, the multilayer structure comprising:
3 a semiconductor/germanium layer;

4 a strained semiconductor layer including a source and a drain
5 provided below the semiconductor/germanium layer, the
6 semiconductor/germanium layer having an aperture;
7 a gate dielectric above the strained semiconductor layer and
8 within the aperture; and
9 a gate conductor within the aperture.

1 9. The multilayer structure of claim 8, further comprising:
2 a spacer in the aperture separating the
3 semiconductor/germanium layer and the gate conductor.

1 10. The multilayer structure of claim 8, further comprising:
2 a silicide layer disposed above the semiconductor/germanium
3 layer.

1 11. A method of making an SMOS structure containing a plurality of
2 transistors, the method comprising:
3 providing a first semiconductor substrate including a base layer,
4 a strained semiconductor layer, and a first oxide layer;
5 attaching a second semiconductor substrate including a second
6 oxide layer to the first oxide layer; and
7 separating the base layer from the first substrate.

1 12. The method of claim 11, wherein a semiconductor/germanium
2 layer is above the strained semiconductor layer.

1 13. The method of claim 12, further comprising:
2 providing an aperture in the semiconductor/germanium layer.

1 14. The method of claim 13, further comprising:

2 doping the strained semiconductor layer through the aperture.

1 15. The method of claim 15, wherein the doping step forms source
2 and drain extensions.

1 16. The method of claim 13, further comprising:
2 providing a gate conductor in the aperture.

1 17. The method of claim 16, further comprising:
2 separating the gate conductor from the silicon/germanium layer
3 with a spacer material.

1 18. The method of claim 12, further comprising:
2 siliciding the semiconductor/germanium layer.

1 19. The method of claim 11, wherein the attaching step is a
2 hydrogen bonding step.